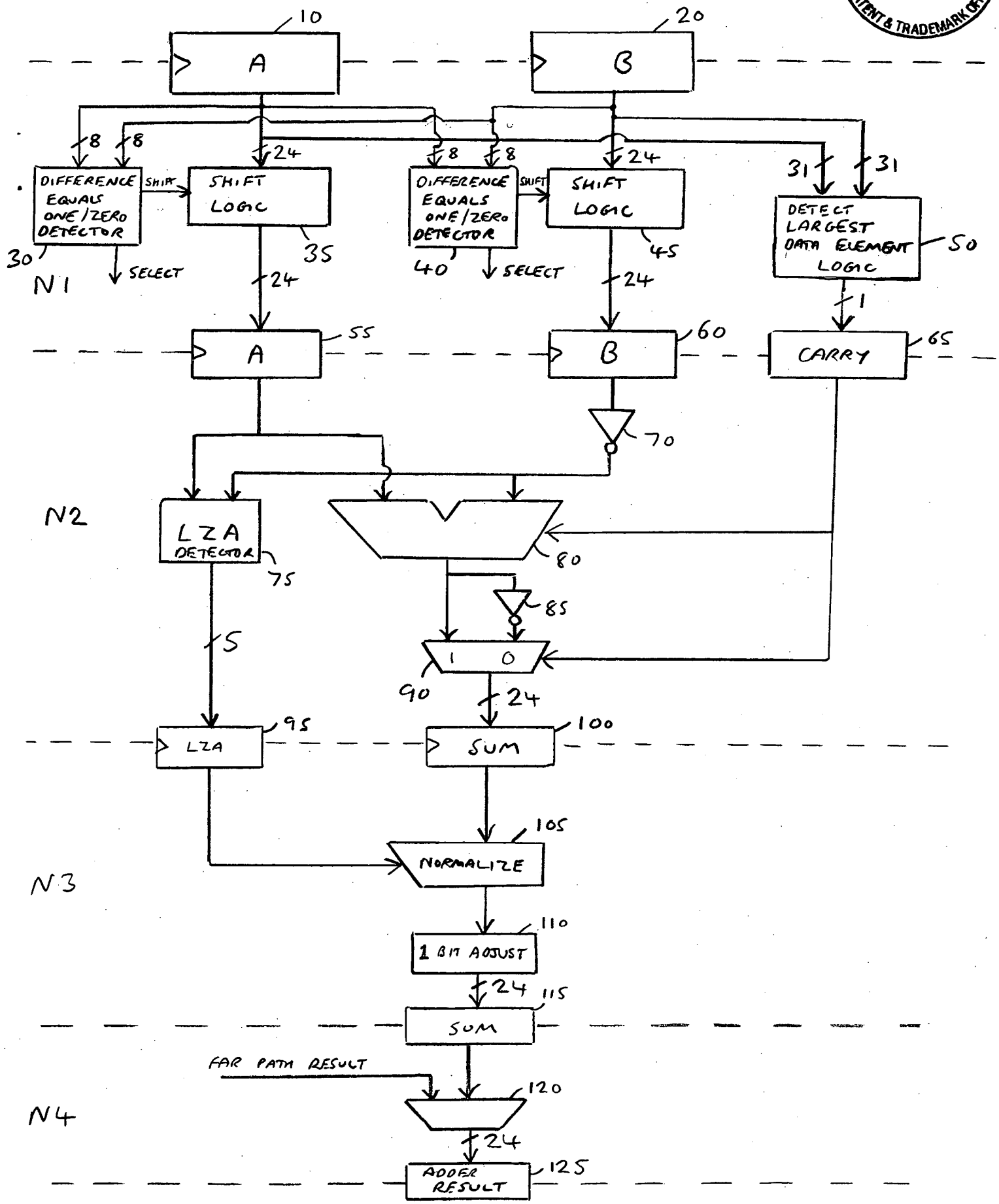

FIG. 1

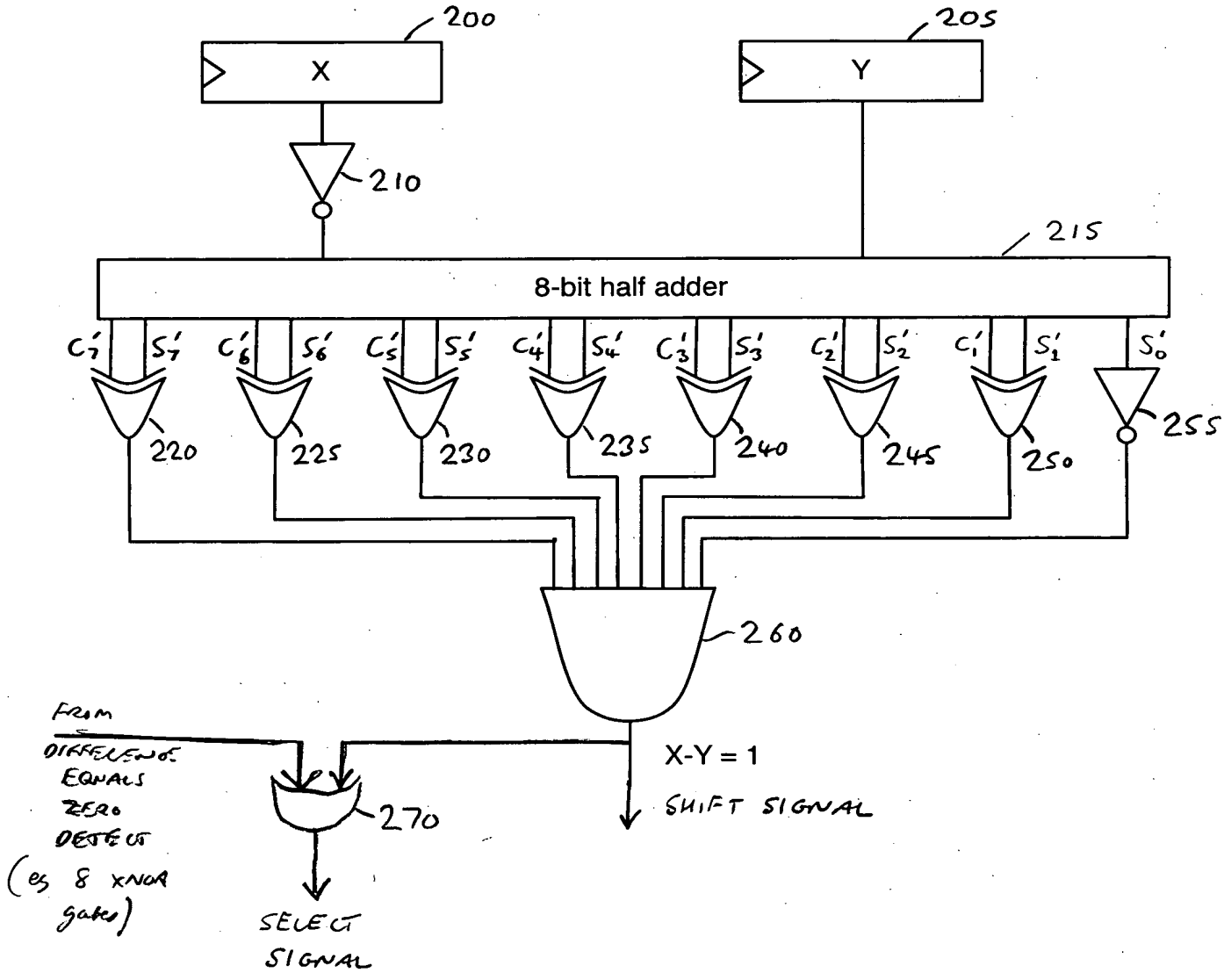
200
X
205
Y
210
215
8-bit half adder
C_7' S_7' C_6' S_6' C_5' S_5' C_4' S_4' C_3' S_3' C_2' S_2' C_1' S_1' S_0'
220
225
230
235
240
245
250
255
260
FROM DIFFERENCE EQUALS ZERO DETECT (eg 8 XNOR gates)
270
SELECT SIGNAL
X-Y = 1
SHIFT SIGNAL

FIG. 2

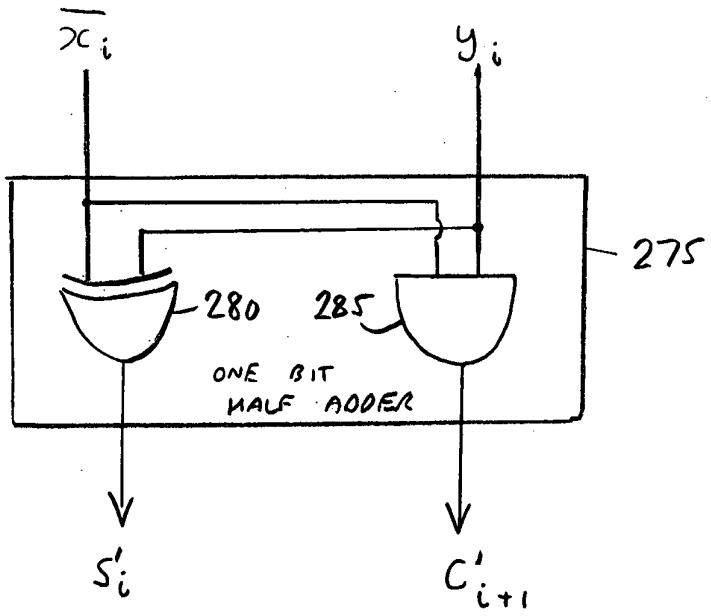

FIG. 3

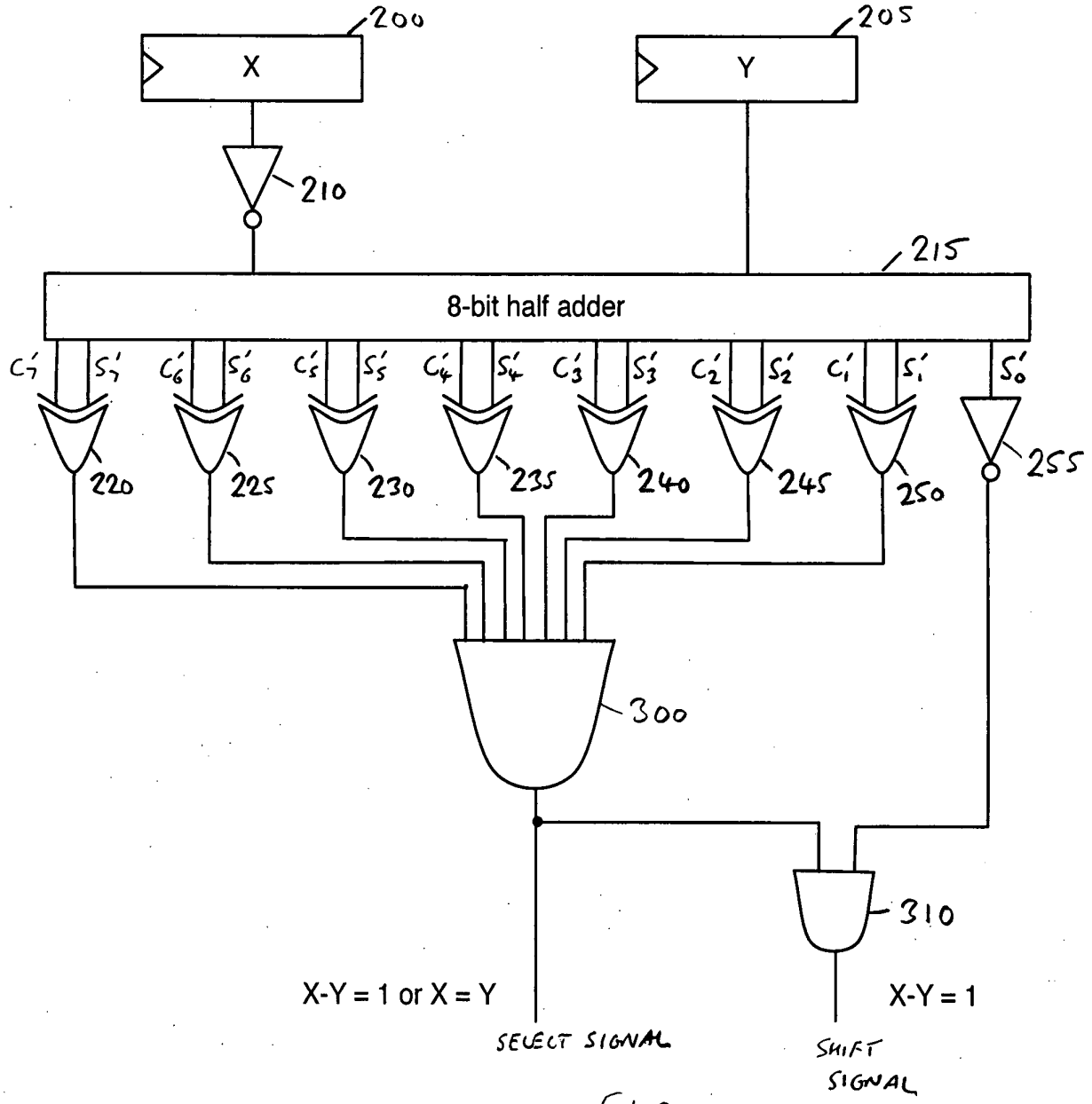
200
X
205
Y
210
215
8-bit half adder
C_7' S_7' C_6' S_6' C_5' S_5' C_4' S_4' C_3' S_3' C_2' S_2' C_1' S_1' S_0'
220
225
230
235
240
245
250
255
300
310
X-Y = 1 or X = Y
SELECT SIGNAL
X-Y = 1
SHIFT SIGNAL

FIG. 4

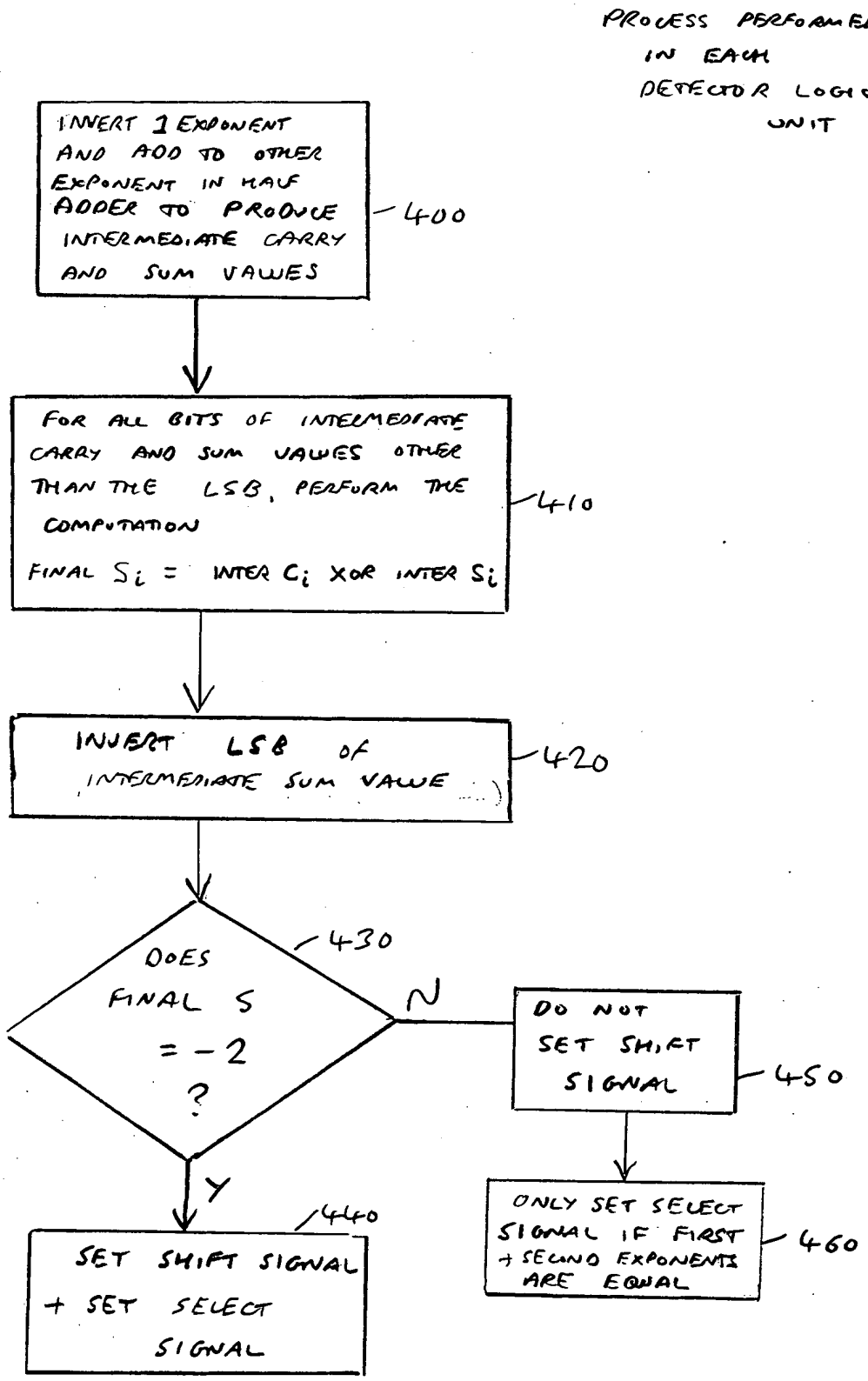
PROCESS PERFORMED IN EACH DETECTOR LOGIC UNIT
INVERT 1 EXPONENT AND ADD TO OTHER EXPONENT IN HALF ADDER TO PRODUCE INTERMEDIATE CARRY AND SUM VALUES
400
FOR ALL BITS OF INTERMEDIATE CARRY AND SUM VALUES OTHER THAN THE LSB, PERFORM THE COMPUTATION
FINAL S_i = INTER C_i XOR INTER S_i
410
INVERT LSB OF INTERMEDIATE SUM VALUE
420
DOES FINAL S = -2 ?
430
N
DO NOT SET SHIFT SIGNAL
450
ONLY SET SELECT SIGNAL IF FIRST + SECOND EXPONENTS ARE EQUAL
460
Y
SET SHIFT SIGNAL + SET SELECT SIGNAL
440

FIG. 5

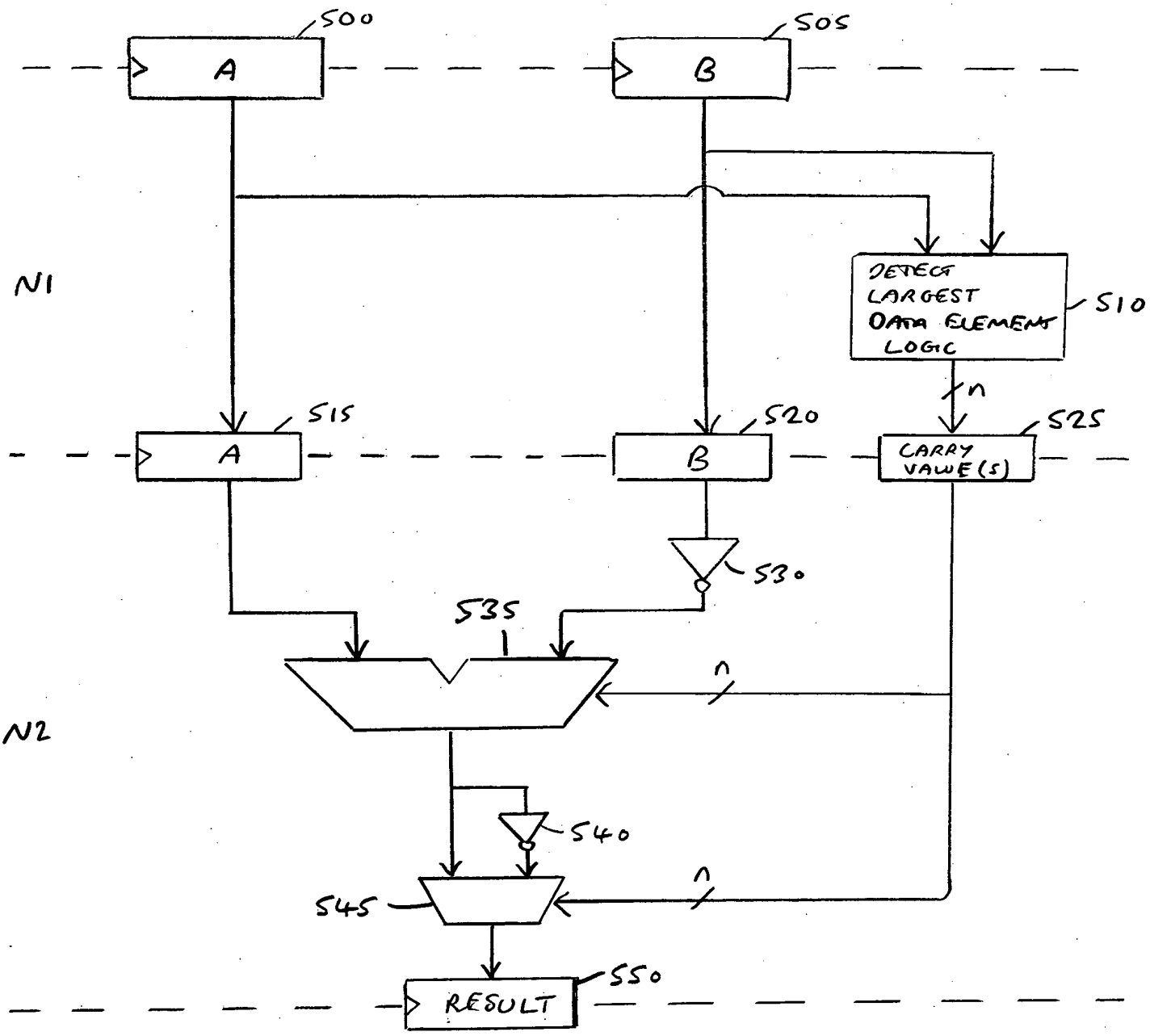
500
A
505
B
N1
DETECT LARGEST DATA ELEMENT LOGIC
510
n
515
A
520
B
525
CARRY VALUE(S)
530
535
n
N2
540
545
n
550
RESULT

FIG. 6

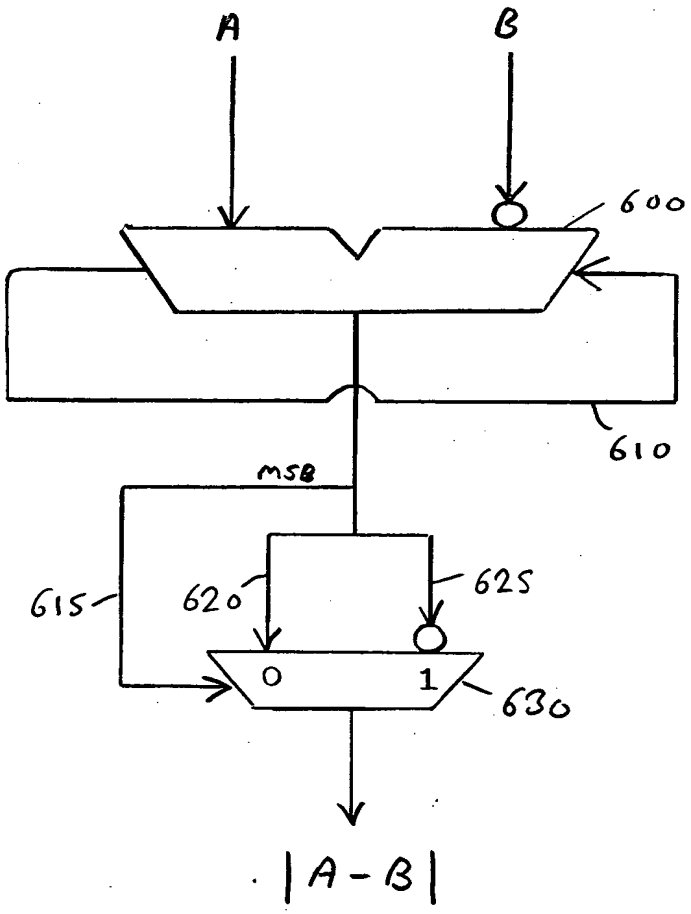

FIG. 7 (PRIOR ART)

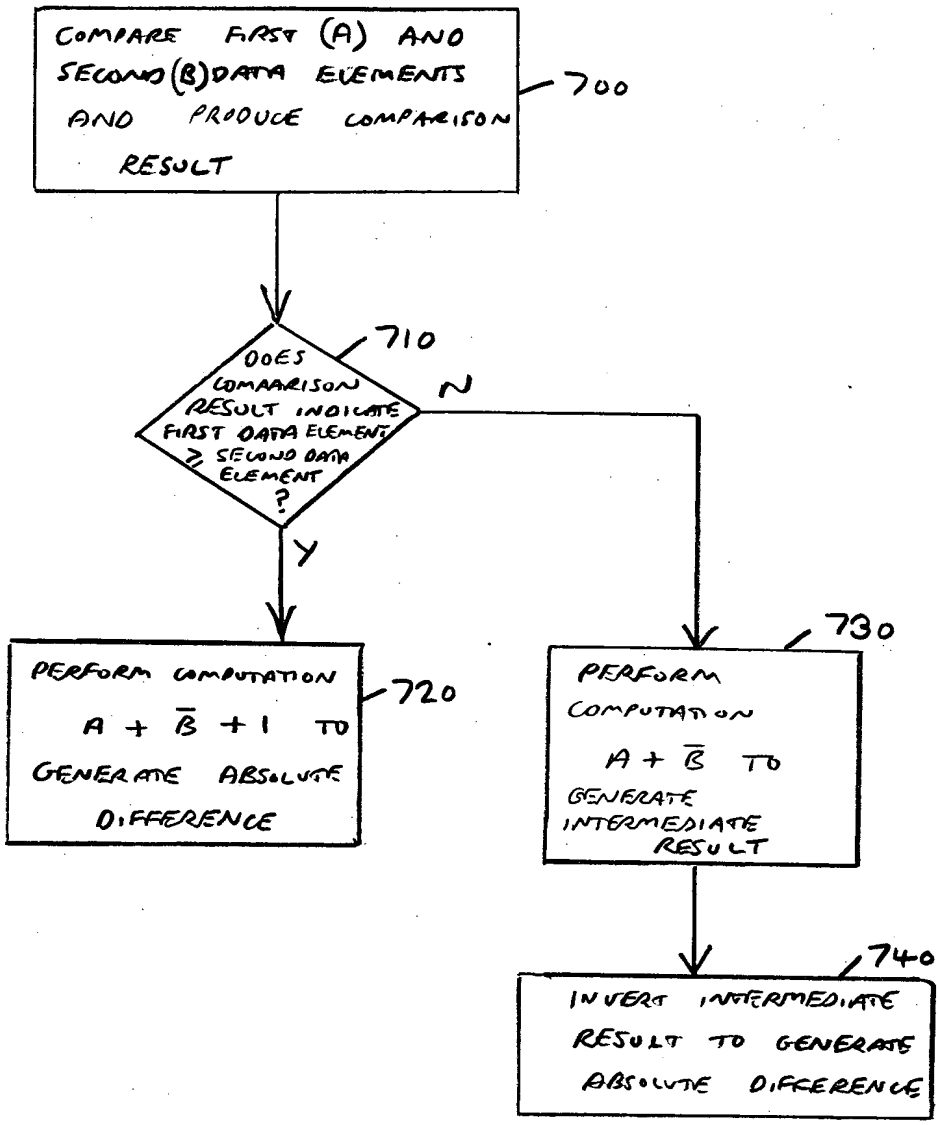
COMPARE FIRST (A) AND SECOND (B) DATA ELEMENTS AND PRODUCE COMPARISON RESULT
700
DOES COMPARISON RESULT INDICATE FIRST DATA ELEMENT ≥ SECOND DATA ELEMENT ?
710
N
Y
PERFORM COMPUTATION A + B̄ + 1 TO GENERATE ABSOLUTE DIFFERENCE
720
PERFORM COMPUTATION A + B̄ TO GENERATE INTERMEDIATE RESULT
730
INVERT INTERMEDIATE RESULT TO GENERATE ABSOLUTE DIFFERENCE
740

FIG. 8